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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/780,606	02/19/2004	Jae-Hee Oh	9862-000026/US	3174

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EXAMINER	
NADAV, ORI	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 08/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/780,606	OH ET AL.
	Examiner	Art Unit
	Ori Nadav	2811

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 August 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8 and 10-22* is/are pending in the application.

4a) Of the above claim(s) *3,4 and 10-22* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2 and 5-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, a first sub-layer formed on the first metal wiring and a second sub-layer formed on the capacitor, the first metal wiring and the first sub-layer, the second sub-layer including a lower layer that is formed between the upper electrode and the first metal wiring, and an upper layer that is formed over the upper electrode, as recited in claim 1, must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will

be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> **The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.**

Claims 1-2 and 5-8 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The claimed limitations of an insulating interlayer includes a first sub-layer formed on the first metal wiring and a second sub-layer formed on the capacitor, the first metal wiring and the first sub-layer, the second sub-layer including a lower layer that is formed between the upper electrode and the first metal wiring, and an upper layer that is formed over the upper electrode, as recited in claim 1, are unclear as to whether the insulating interlayer is one of the first or second insulating layers, what is the structural relationship between the insulating interlayer and the first or second insulating layers, how one layer (an interlayer and a second sub-layer) can include plurality of layers.

The claimed limitation of a first metal wiring having a first metal thickness, as recited in claim 1, is unclear as to the first metal thickness is in the x direction or the y direction (i.e. height) of the first metal wiring.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-2 and 5-8, insofar as in compliance with 35 U.S.C. 112, are rejected under 35 U.S.C. 103(a) as being unpatentable over Okumura et al. (6,163,046) in view of Suwanai et al. (5,389,558).

Regarding claim 1, Okumura et al. teach in figures 35 and 38 and related text a semiconductor device comprising:

a cell array region 3 formed in a semiconductor substrate and including a capacitor having a lower electrode and an upper electrode, the lower electrode having a lower electrode height;

a peripheral circuit region 4 formed in the semiconductor substrate and including a first metal wiring, the first metal wiring 21B having a first metal thickness, and having a lower surface in a substantially planar orientation with a lower surface of the lower electrode 16;

a first insulating layer formed on the cell array region and the peripheral circuit region and having openings; and

a second insulating layer formed on the first insulating layer, the first metal wiring being arranged in the second insulating layer,

Okumura et al. do not teach an insulating interlayer includes a first sub-layer formed on the first metal wiring and a second sub-layer formed on the capacitor, the first metal wiring and the first sub-layer, the second sub-layer including a lower layer that is formed between the upper electrode and the first metal wiring, and an upper layer that is formed over the upper electrode.

Suwanai et al. teach an insulating interlayer 51 includes a first sub-layer formed on the first metal wiring and a second sub-layer formed on the capacitor, the first metal wiring and the first sub-layer, the second sub-layer including a lower layer that is formed between the upper electrode and the first metal wiring, and an upper layer that is formed over the upper electrode.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use an insulating interlayer which includes a first sub-layer formed on the first metal wiring and a second sub-layer formed on the capacitor, the first metal wiring and the first sub-layer, the second sub-layer including a lower layer that is formed between the upper electrode and the first metal wiring, and an upper layer that is formed over the upper electrode in Okumura et al.'s device in order to improve the protection to the device.

Regarding claims 2 and 5-8, Okumura et al. teach in figures 35 and 38 and related text a first conductive plug extending through the first insulating layer to connect the lower electrode to the semiconductor substrate; and

a second conductive plug extending through the first insulating layer to connect the first metal wiring to the semiconductor substrate.

first gate structures formed in the cell array region, the first insulating layer being formed on the first gate structures;

second gate structures formed in the peripheral region, the first insulating layer being formed on the second gate structures;

a first storage node contact hole and a first bit line contact hole formed through the first insulating layer for exposing a first surface of the substrate in the cell array region;

first metal contact holes formed through the first insulating layer for exposing the first and second gate structures and a second surface of the substrate in the peripheral region;

conductive plugs formed in the first storage node contact hole, the first bit line contact hole and the first metal contact hole, the first metal wiring being in electrical contact with the conductive plug in the first metal contact hole;

a capacitor formed in the second insulating layer in the cell array region, the capacitor being in electrical contact with the conductive plug in the first storage node contact hole;

an insulating interlayer 20 formed on the capacitor, the first metal wiring and the second insulating layer; and

a second metal wiring 32 formed on the insulating interlayer in the peripheral region, the second metal wiring being electrically connected to the first metal wiring,

wherein the peripheral region includes at least one of core circuitry peripheral circuitry and logic circuitry,

wherein the capacitor has a metal/insulator/metal structure, and

a bit line formed on the insulating interlayer and electrically connected to the conductive plug in the first bit line contact hole through a second bit line contact hole formed through the insulating interlayer, wherein the bit line and the second metal wiring are formed from a single metal layer,

wherein the insulating interlayer includes a first sub-layer formed on the first metal wiring and a second sub-layer formed on the capacitor, the first metal wiring and the first sub-layer.

Response to Arguments

Applicant's arguments with respect to claims 1-2 and 5-8 have been considered but are moot in view of the new ground(s) of rejection.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ori Nadav whose telephone number is 571-272-1660. The examiner can normally be reached between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Loke can be reached on 571-272-1657. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

O.N.
8/19/05

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PRIMARY EXAMINER
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